SPECIFICATION AMENDMENTS

Please replace the paragraph **[0020]** on page 6 of the Specification with the following paragraph:

[0020] A control and adjudication logic circuit 50 chooses the most likely timing hypothesis. The control and adjudication logic circuit 50 provides a detector select control signal 54 and a data output control signal 56. A select switch 60 receives outputs from the data detector array 42 and the detector select control signal 54. Using the detector select control signal 54, the selector switch 60 ~~outputs~~ selects the output from the data detector array 42 that corresponds to the most likely timing hypothesis that is identified by the control and adjudication logic circuit 50. The output of the select switch 60 is connected to a threshold test circuit 62. The threshold test circuit 62 compares the selected signal to a threshold value, such as zero. If the selected signal is greater than the threshold value, the threshold test circuit 62 outputs a mark. If the selected signal is less than the threshold value, then the threshold test circuit 62 outputs a space. The output of the threshold test circuit 62 is connected to an output control circuit 64. The output control circuit 64 passes zero, one or two symbols depending upon the data output control signal 56 that is received from the control and adjudication logic circuit 50 as will be described further below.

Please replace the paragraph **[0021]** beginning on page 6 of the Specification with the following paragraph:

[0021] Referring now to figures 3 and 4, an exemplary implementation of a maximum likelihood bit synchronization circuit 100, according to the invention, is shown. For purposes of clarity, reference numerals from figure 2 have been used where appropriate to identify similar elements. The detected signal 32 from figure 2 is input to the average level estimator 34 that is implemented using a single pole, recursive, infinite impulse response (IIR) filter 102 in one embodiment. The detected signal 32 is an OOK detected envelope signal in the example discussed above. However, as will be appreciated by those skilled in the art, the signal 32 can be any binary level signal suitable for the purposes described herein. An output of the filter 102 is input to an inverting input of the summer 36. The OOK detected envelope signal 32 is also input to a non-inverting input of the summer 36. The summer 36 generates the antipodal signal that is input to maximum likelihood bit synchronization subcircuits 106A and 106B.

Please replace the paragraph **[0023]** on page 7 of the Specification with the following paragraph:

[0023] Referring now to figures 3 and 5, an alternate exemplary implementation of the maximum likelihood bit synchronizer ~~100'~~ is shown. The alternate maximum likelihood bit synchronizer ~~100'~~ implements the averaging circuit 48 in a different manner by replacing the sliding-window summers 48-1, 48-2, ..., 48-6 of figure 4 with single pole, unity-gain, low pass filters 120-1, 120-2, ..., 120-6 of

figure 5.

Please replace the paragraph **[0028]** on page 10 of the Specification with the following paragraph:

[0028] The maximum likelihood bit synchronizer according to the present invention produces a true maximum likelihood symbol timing decision. The maximum likelihood bit synchronizer uses an open-loop, feedforward configuration. Additional timing hypotheses and control and adjudication logic are used to detect relative received symbol and sampling clock drift. The maximum likelihood bit synchronizer also prevents bit slippage without the need for a numerically controlled oscillator (NCO) and a feedback loop.